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EXAMINER	
JOHNSON, CARLTON	

ART UNIT	PAPER NUMBER
2436	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/789,311	SHANTZ ET AL.	
	Examiner	Art Unit	
	CARLTON V. JOHNSON	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1-24-2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 1/24/2011, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Nasser Moazzami/

Supervisory Patent Examiner, Art Unit 2436

2. Claims **1 - 67** are pending. Claims **1, 21, 38, 53, 66, 67** are independent. This application was filed on 2-27-2004.

Response to Arguments

3. Applicant's arguments have been fully considered and they were partially persuasive, therefore new grounds of rejection have been entered. .

3.1 Applicant argues the Huppenthal and Hinds prior art references.

Huppenthal and Hinds are no longer used as grounds of rejection.

Takahashi is used to disclose a processor capability of performing multiple pipeline operations from a single instruction. This capability is part of the processor architecture or processor instruction set. Takahashi disclose a system capable of performing cryptographic type operation such as encryption and decryption of data. Takahashi discloses the capability to use the high order bit from previous operations in subsequent operations. (see Takahashi paragraph [0009], lines 1-3: provides multi-function processor architecture capable of performing mathematic operations (implies arithmetic operations are part of system architecture or instruction set; paragraph [0017], lines 1-8: system for encrypting and decrypting data; paragraph [0017], lines 1-19: pipeline storage processing stage iteratively computing a running partial product using one or more received operands a predetermined number of times; post processing stage to receive final partial product and compute result; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1, 4 - 10, 19, 21 - 26, 36, 38 - 42, 48, 52 - 60, 62, 66, 67** are rejected under 35 U.S.C. 102(e) as being anticipated by **Takahashi et al.** (US PGPUB No. **20020194237**)

With Regards to Claims 1, 21, 38, 53, 66, 67, Takahashi discloses a method implemented in a device supporting a public-key cryptography application, the method comprising:

a first arithmetic circuit comprising a first plurality of arithmetic structures feeding back high order bits of a previously executed single arithmetic instruction of a processor instruction set in the public-key cryptography application, generated by the first arithmetic circuit, (see Takahashi paragraph [0009], lines 1-3: provides multi-function processor architecture capable of performing mathematic operations (implies arithmetic operations are part of system architecture or instruction set and pipeline processing initiated by a single instruction); paragraph [0017], lines 1-8: system for encrypting and decrypting data; includes an encryption/decryption engine operable to encrypt received data paragraph [0017], lines 8-14: one or more processor are operable to receive one or more operands and compute a result)

a second arithmetic circuit generating a first partial result of a currently executing

single arithmetic instruction in the public-key cryptography application, wherein the currently executing single arithmetic instruction does not include an explicit source operand for specifying the high order bits, the first partial result representing the high order bits summed with low order bits of a result of a first number multiplied by a second number, the summing of the high order bits being performed during multiplication of the first number and the second number, the summing and at least a portion of the multiplication being performed in the second arithmetic circuit; (Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion and receives operands stored in operand storage portion; paragraph [0017], lines 1-19: pipeline storage processing (multiplication, summation) stage iteratively computing a running partial product using one or more received operands a predetermined number of times; post processing stage to receive final partial product and compute result; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

storing the first partial result; (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes registers) and

using the stored first partial result in a subsequent computation in the public-key cryptography application. (see Takahashi paragraph [0017], lines 1-19: encryption/decryption engine operable to encrypt/decrypt received data; pipeline

processing operable to receive operands; iteratively computing a running partial product using the one or more received operands)

With Regards to Claim 4, Takahashi discloses the method as recited in claim 1, further comprising feeding back the high order bits through a register to the second arithmetic circuit. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; paragraph [0044], lines 1-14: carry-save processor (operations) feeds back highest order bit to next operation in pipeline)

With Regards to Claim 5, Takahashi discloses the method as recited in claim 1 furtrher comprising generating a second partial result of the currently executing single arithmetic instruction in the first arithmetic circuit, the second partial result representing the high order bits of the multiplication result of the first number multiplied by the second number. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes at least five registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; paragraph [0044], lines 1-14: carry-save feeds back highest order bit to next operation in pipeline)

With Regards to Claim 6, Takahashi discloses the method as recited in claim 1 further comprising: discloses generating a second partial result of the currently executing single arithmetic instruction, the second partial result representing the high order bits of the

multiplication result of the first number multiplied by the second number summed with the high order bits of the executed arithmetic instruction previously executed single arithmetic instruction. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes at least five registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; paragraph [0044], lines 1-14: carry-save feeds back highest order bit to next operation in pipeline)

With Regards to Claim 7, Takahashi discloses the method as recited in claim 6 further comprising supplying values generated in one or more most significant columns of the second arithmetic structures to one or more least significant columns of the first arithmetic structures while generating the first and second partial results. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 8, Takahashi discloses the method as recited in claim 5 further comprising generating of the first and second partial result is in response to execution of a currently executing single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion; iteratively computes a running partial product predetermined number of times using received operands)

With Regards to Claim 9, Takahashi discloses the method as recited in claim 6 further comprising generating of the first and second partial result is in response to execution of a currently executing single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion; iteratively computes a running partial product predetermined number of times using received operands; (pipeline processing is a single instructions))

With Regards to Claim 10, Takahashi discloses the method as recited in claim 1 wherein at least one of the first and second pluralities of arithmetic structures comprises a plurality of carry save adder tree columns. (see Takahashi paragraph [0043], lines 6-13: pipeline processing stage includes carry-save processors (4 processors))

With Regards to Claim 19, Takahashi discloses the method as recited in claim 1 wherein feeding back high order bits of the currently executing arithmetic instruction from the first arithmetic circuit to the second arithmetic circuit for use with execution of a subsequent single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion; iteratively computes a running partial product predetermined number of times using received operands; (pipeline processing is a single instructions))

With Regards to Claim 22, Takahashi discloses the method as recited in claim 21,

further comprising feeding back the high order bits through a register to the second arithmetic circuit. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes at least five registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion)

With Regards to Claim 23, Takahashi discloses the method as recited in claim 21. the first arithmetic circuit generating a second partial result of the currently executing arithmetic instruction, the second partial result representing the high order bits of the multiplication result of the first number multiplied by the second number. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 24, Takahashi discloses the method as recited in claim 21. generating a second partial result of the currently executing arithmetic instruction, the second partial result representing the high order bits of the multiplication result of the first number multiplied by the second number summed with the high order bits of the previously executed arithmetic instruction and the third number. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times

using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 25, Takahashi discloses the method as recited in claim 24 wherein supplying values generated in one or more most significant columns of the second arithmetic structures to one or more least significant columns of the first arithmetic structures while generating the first and second partial results. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 26, Takahashi discloses the method as recited in claim 23 wherein generating of the first and second partial result is in response to execution of a single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage; pipeline processing iteratively computes a running partial product a predetermined number of times using received operands)

With Regards to Claim 36, Takahashi discloses the method as recited in claim 21

further comprising feeding back high order bits of the currently executing arithmetic instruction from the first arithmetic circuit to the second arithmetic circuit for use with execution of a subsequent single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 39, Takahashi discloses the processor as recited in claim 38. the first arithmetic structures are configured to generate a second partial result of the arithmetic instruction, the second partial result representing the high order bits of the arithmetic operation. (see Takahashi paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 40, Takahashi discloses the processor as recited in claim 39. the second arithmetic structures are further configured to supply values generated in one or more most significant columns of the second arithmetic structures to one or more least significant columns of the first arithmetic structures while generating the first and second partial results. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product

a predetermined number of times using received operands; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 41, Takahashi discloses the processor as recited in claim 39, wherein the first and second arithmetic structures are configured to generate of the first and second partial results in response to execution of a single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion coupled to operand storage portion; iteratively computes running partial product a predetermined number of times using received operands)

With Regards to Claim 42, Takahashi discloses the processor as recited in claim 38, further comprising a register coupled to the first and second arithmetic structures to supply the high order bits to the second arithmetic structures. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes at least five registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion)

With Regards to Claim 48, Takahashi discloses the processor as recited in claim 38. at least one of the first and second pluralities of arithmetic structures comprises a plurality of carry save adder tree columns. (see Takahashi paragraph [0043], lines 6-

13: pipeline processing stage includes multiple carry-save processors (4 processors))

With Regards to Claim 52, Takahashi discloses the processor as recited in claim 38, wherein the processor is a general purpose processor. (see Takahashi paragraph [0003], lines 1-5: processor for performing operations)

With Regards to Claim 54, Takahashi discloses the processor as recited in claim 53, wherein the first arithmetic structures are further configured to generate a second partial result of the arithmetic instruction, the second partial result representing the high order bits of the arithmetic operation. (Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save (a0 position); second carry-save (a1 position,...))

Pipeline operation implies that arithmetic operations are performed as iterative steps with the operand storage portion used to implicit transfer the operands of previous operations to the next pipeline operations.

With Regards to Claim 55, Takahashi discloses the processor as recited in claim 54, wherein the second arithmetic structures are further configured to generate values in one or more most significant columns and to supply them to one or more least significant columns of the first arithmetic structures while generating the first and second partial results. (Takahashi paragraph [0038], lines 1-7: pipeline processing portion is

coupled to operand storage portion; paragraph [0044], lines 1-14: receive bit stored in the current highest order position; first carry-save processor (a0 position); second carry-save processor (a1 position); third carry-save processor (a2); ...)

With Regards to Claim 56, Takahashi discloses the processor as recited in claim 54, wherein the first arithmetic structures are configured to generate of the first and second partial result in response to execution of a single arithmetic instruction. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; pipeline computes a running partial product a predetermined number of times; at least a portion of the one or more received operands in each iteration; (implies a single arithmetic execution initiate an iteration of arithmetic operations))

With Regards to Claim 57, Takahashi discloses the processor as recited in claim 53, a further comprising a register coupled to the first and second arithmetic structures to supply the high order bits to the second arithmetic structures. (see Takahashi paragraph [0041], lines 9-20: operand storage portion includes at least five registers; paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion)

With Regards to Claim 58, Takahashi discloses the processor as recited in claim 53, further comprising an adder circuit configured to receive the first partial result and to generate a non redundant representation of the first partial result and a carry out value. (see Takahashi paragraph [0012], lines 1-4: performing a carry-save add of at least a

first operand)

With Regards to Claim 59, Takahashi discloses the processor as recited in claim 58 wherein the adder circuit is further configured to feed the carry out value back to itself as an input. (see Takahashi paragraph [0045], lines 1-11: carry-save processor are in a ring configuration; output of fourth carry-save processor is input to first carry-save processor; (carry out value eventually input to itself))

With Regards to Claim 60, Takahashi discloses the processor as recited in claim 58, wherein the adder circuit is further configured to feed the carry out value back to the second arithmetic structures. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; iteratively computes a partial product a predetermined number of times using a portion of one or more received operands)

With Regards to Claim 62, Takahashi discloses the processor as recited in claim 53, wherein at least one of the first and second arithmetic structures comprises carry save adder tree columns. (see Takahashi paragraph [0012], lines 1-5: carry-save processor for performing carry-save add of at least a first operand, second operand, third operand)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **2, 3, 15 - 18, 27 - 29, 35, 43 - 46** are rejected under 35 U.S.C. 102(e) as being unpatentable over **Takahashi** in view of **Lasher et al.** (US Patent No. **4,863,247**).

With Regards to Claim 2, Takahashi discloses the method as recited in claim 1, wherein the high order bits are fed back. (see Takahashi paragraph [0038, lines 1-7: : pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forward to the next operand); paragraph [0044], lines 1-14: carry-save operation utilizes current high order bit position)

Takahashi does not specifically disclose redundant number representation.

However, Lasher discloses wherein the result is in redundant number representation. (see Lasher col. 6, lines 6-9; col. 6, lines 16-18: redundant number representations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for a result in redundant number representation as taught by Lasher. One of ordinary skill in the art would have been motivated to employ the teachings of Lasher in order that fully parallel carry-free operation is provided for with reduced complexity. (see Lasher col. 2, lines 57-62)

With Regards to Claim 3, Takahashi discloses the method as recited in claim 2 includes sum and carry bits.

Takahashi does not specifically disclose redundant number representation.

However, Lasher discloses wherein the result is in redundant number representation. (see Lasher col. 6, lines 6-9; col. 6, lines 16-18: redundant number representations)

Motivation for Lasher to disclose redundant number representation is as stated in Claim 2 above.

With Regards to Claim 15, Takahashi discloses the method as recited in claim 1 wherein the first partial result. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands)

Takahashi does not specifically disclose redundant number representation.

However, Lasher discloses wherein the result is in redundant number representation. (see Lasher col. 6, lines 6-9; col. 6, lines 16-18: redundant number representations)

Motivation for Lasher to disclose redundant number representation is as stated in Claim 2 above.

With Regards to Claim 16, Takahashi discloses the method as recited in claim 15 further comprising supplying the first partial result to an adder circuit to generate the first partial result and a carry out value. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times

using received operands)

Takahashi does not specifically disclose redundant number representation. However, Lasher discloses wherein the result is a non redundant representation. (see Lasher col. 6, lines 6-9; col. 6, lines 16-18: redundant number representations) Motivation for Lasher to disclose redundant number representation is as stated in Claim 2 above.

With Regards to Claim 17, Takahashi discloses the method as recited in claim 16 further comprising feeding back the carry out value to the adder circuit. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forwards high order bits using operand))

With Regards to Claim 18, Takahashi discloses the method as recited in claim 16 further comprising feeding back the carry out value to the second arithmetic circuit. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forwards high order bits using operand))

With Regards to Claim 27, Takahashi discloses the method as recited in claim 21 further comprising supplying the first partial result to an adder circuit to generate a non redundant representation of the first partial result and a carry out value. (see Takahashi paragraph [0017], lines 11-19: each processor includes operand storage, pipeline processing portion, post-processing stage; pipeline processing iteratively computing a running partial product using one or more received operands)
Takahashi does not specifically disclose redundant number representation.
However, Lasher discloses wherein the result is a non redundant number representation. (see Lasher col. 6, lines 6-9; col. 6, lines 16-18: redundant number representations)
Motivation for Lasher to disclose redundant number representation is as stated in Claim 2 above.

With Regards to Claim 28, Takahashi discloses the method as recited in claim 27 further comprising feeding back the carry out value to the adder circuit. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forwards high order bits using operand))

With Regards to Claim 29, Takahashi discloses the method as recited in claim 27 further comprising feeding back the carry out value to the second arithmetic structures. (see Takahashi paragraph [0017], lines 11-19: each processor includes operand storage, pipeline processing portion, post-processing stage; pipeline processing iteratively computing a running partial product using one or more received operands)

With Regards to Claim 35, Takahashi discloses the method as recited in claim 21 wherein the high order bits. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forwards high order bits using operand))
Lasher discloses the result is in redundant number representation as stated in Claim 2 above.

With Regards to Claim 43, Takahashi discloses the processor as recited in claim 38, wherein the first partial result. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands)
Takahashi does not specifically disclose redundant number representation.
Lasher discloses the result is in redundant number representation as stated in Claim 2 above.

With Regards to Claim 44, Takahashi discloses the processor as recited in claim 43 further comprising an adder circuit configured to receive the first partial result and to generate a non redundant representation of the first partial result and a carry out value. (see Takahashi paragraph [0038, lines 1-7: pipeline processing; iteratively computes a partial product a predetermined number of times using received operands; paragraph [0012], lines 1-5; paragraph [0043], lines 6-13: pipeline processing stage includes a carry-save processor; (carry-save implies high order bits are carried forwards high order bits using operand))

With Regards to Claim 45, Takahashi discloses the processor as recited in claim 44 further comprising an adder circuit configured to feed the carry out value back to itself as an input. (see Takahashi paragraph [0045], lines 1-11: carry-save processor are in a ring configuration; output of fourth carry-save processor is input to first carry-save processor; (carry out value eventually input to itself))

With Regards to Claim 46, Takahashi discloses the processor as recited in claim 44 further comprising an adder circuit configured to feed the carry out value back to the second arithmetic structures. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage portion; iteratively computes a partial product a predetermined number of times using a portion of one or more received operands)

7. Claims **11, 20, 30, 31, 37, 47, 61** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takahashi** and further in view of **Stribaek et al.** (US Patent No. **7,181,484**).

With Regards to Claim 11, Takahashi discloses the method as recited in claim 1, further comprising at least one of the first and second pluralities of arithmetic structures. (see Takahashi paragraph [0017], lines 11-19: each processor includes operand storage, pipeline processing portion, post-processing stage; pipeline processing iteratively computing a running partial product using one or more received operands) Takahashi does not specifically disclose whereby a plurality of Wallace tree columns. However, Stribaek discloses wherein further comprises a plurality of Wallace tree columns. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for usage of Wallace tree multiplication as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 20, Takahashi discloses the method as recited claim 1, further comprising storing the high order bits.
Takahashi does not specifically disclose whereby an extended carry register.

However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree; col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for usage of extended carry operations as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 30, Takahashi discloses the method as recited in claim 21, wherein at least one of the first and second pluralities of arithmetic structures. Takahashi does not specifically disclose a plurality of Wallace tree columns. However, Stribaek discloses wherein further comprises a plurality of Wallace tree columns. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree; col. 2, line 66 - col. 3, line 6: public key cryptographic calculations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for usage of Wallace tree multiplication as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 31, Takahashi discloses the method as recited in claim 21,

wherein at least one of the first and second pluralities of arithmetic structures.

Takahashi does not specifically disclose carry save adder tree columns.

However, Stribaek discloses wherein further comprises a plurality of adder tree columns. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree; col. 5, lines 41-45: extended carry operations; col. 7, lines 31-37; col. 9, lines 10-14: carry-save adder; col. 2, line 66 - col. 3, line 6: public key cryptographic calculations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for usage of Wallace tree multiplication as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 37, Takahashi discloses the method as recited in claim 21, further comprising storing the high order bits.

Takahashi does not specifically disclose an extended carry register.

However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree; col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for an extended carry register as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and

increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 47, Takahashi discloses the processor as recited in claim 38, wherein at least one of the first and second pluralities of the arithmetic structures. Takahashi does not specifically disclose whereby a plurality of Wallace tree columns. However, Stribaek discloses wherein further comprises a plurality of Wallace tree columns. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for a plurality of Wallace tree columns as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

With Regards to Claim 61, Takahashi discloses the processor as recited in claim 53, wherein at least one of the first and second arithmetic structures.
Huppenthal does not specifically disclose Wallace tree columns.
However, Stribaek discloses wherein further comprises a Wallace tree column. (see Stribaek col. 9, lines 10-24; col. 9, lines 37-39: Wallace tree)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for Wallace tree columns as taught by Stribaek. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and

increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

8. Claims **12 - 14, 32 - 34, 49 - 51, 63 - 65** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takahashi** and further in view of **Chen et al.** (US Patent No. **6,687,725**).

With Regards to Claim 12, Takahashi discloses the method as recited in claim 1, wherein at least one of the first and second pluralities of arithmetic structures is usable to perform integer multiplication.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein to perform XOR multiplication. (see Chen2 col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi to perform XOR multiplication as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 13, Takahashi discloses the method as recited in claim 12, further comprising a logical circuit in at least one of the first and second arithmetic circuits supplying a variable value for integer multiplication mode that varies according

to inputs supplied to the logical circuit if in integer multiplication mode, to thereby ensure a result unaffected by carry logic performing carries in integer multiplication mode. (see Takahashi paragraph [0038], lines 1-7: pipeline processing portion is coupled to operand storage; pipeline processing iteratively computes a running partial product a predetermined number of times using received operands; paragraph [0016]: arithmetic operations performed with integers)

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein supplying a fixed value if in XOR multiplication mode and to thereby ensure a result is determined in XOR multiplication. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Chen to support XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 14, Takahashi discloses the method as recited in claim 13 wherein the logical circuit operates as a majority circuit in integer multiplication mode.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein outputs a zero in the XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi to support XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 32, Takahashi discloses the method as recited in claim 21, wherein at least one of the first and second pluralities of arithmetic structures is usable to perform integer multiplication.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein perform both integer and XOR multiplication. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi to perform XOR multiplication as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 33, Takahashi discloses the method as recited in claim 32 wherein a logic circuit in at least one of the first and second pluralities of arithmetic

structures supplying a variable value that varies according to inputs supplied to the logical circuit if in integer multiplication mode, to thereby ensure a result unaffected by carry logic performing carries in integer multiplication mode.
Takahashi does not specifically disclose XOR operations.
However, Chen discloses wherein supplying a fixed value if in XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 34, Takahashi discloses the method as recited in claim 33 wherein the logic circuit operates as a majority circuit in integer multiplication mode.
Takahashi does not specifically disclose XOR operations.
However, Chen discloses wherein outputs a zero in the XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition,

multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 49, Takahashi discloses the processor as recited in claim 38, wherein at least one of the first and second pluralities of arithmetic structures is configured to selectively perform one of integer multiplication according to a control signal.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein to selectively perform XOR multiplication. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 50, Takahashi discloses the processor as recited in claim 49 further comprising a plurality of logic circuits in the first and second pluralities of arithmetic structures, each logic circuit responsive to the control signal to supply a variable output value in integer multiplication mode, the variable output value varying according to values of inputs supplied to the logic circuit, to thereby ensure a result

unaffected by carry logic generating carries in integer multiplication mode.

Takahashi does not specifically disclose XOR multiplication mode.

However, Chen discloses to supply a fixed output value in XOR multiplication mode and ensure a result is determined in XOR multiplication mode a fixed output value in XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for XOR multiplication mode as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 51, Takahashi discloses the processor as recited in claim 50, wherein the logical circuit is configured to operate as a majority circuit in integer multiplication mode.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein to output a zero in XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi to output a zero in XOR multiplication mode as taught by Chen2. One of ordinary skill in the art would have been motivated to employ the teachings of Chen2 in order to provide

an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen2 col. 3, lines 17-21)

With Regards to Claim 63, Takahashi discloses the processor as recited in claim 53, wherein the arithmetic structures are configured to selectively perform one of integer multiplication according to a control signal.
Takahashi does not specifically disclose XOR multiplication.
However, Chen2 discloses wherein to perform XOR multiplication. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi for XOR multiplication as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 64, Takahashi discloses the processor as recited in claim 63. Hinds discloses a plurality of logic circuits in at least one of the first and second pluralities of arithmetic structures, each logic circuit responsive to the control signal to supply a variable output value in integer multiplication mode, the variable output value varying according to values of inputs supplied to the logic circuit, to thereby ensure a

result is unaffected by carry logic generating carries in integer multiplication mode as stated in Claim 1 above.

Huppenthal does not specifically disclose XOR operations.

However, Chen discloses wherein to supply a fixed output value in XOR multiplication mode and to thereby ensure a result is determined in XOR multiplication mode. (see Chen col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Takahashi to support XOR operations as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

With Regards to Claim 65, Takahashi discloses the processor as recited in claim 64, wherein the logical circuit is configured to operate as a majority circuit in integer multiplication mode.

Takahashi does not specifically disclose XOR operations.

However, Chen discloses wherein to output a zero in the XOR multiplication mode. (see Chen2 col. 4, line 64 - col. 5, line 2; col. 15, lines 29-31: XOR operations)

It would have been obvious to one of ordinary skill in the art to modify Chen and to output a zero in the XOR multiplication mode as taught by Chen. One of ordinary skill in the art would have been motivated to employ the teachings of Chen in order to

provide an arithmetic circuit which can perform all arithmetic operations in the finite field, including addition, multiplication, division, exponentiation and inverse multiplication. (see Chen col. 3, lines 17-21)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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CVJ
March 14, 2011

/Nasser Moazzami/

Supervisory Patent Examiner, Art Unit 2436